Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method comprising:

predicting a next micro-operation address;

storing the predicted address into a first memory;

retrieving the predicted address from the first memory;

accessing a second memory at the ~~retreived~~ retrieved address to get a next micro-operation including a plurality of bits, wherein the next micro-operation indicates whether a jump present with at least two jump bits;

determining whether the micro-operation address is correctly predicted by checking the two least significant bits of the next micro-operation address to determine if a jump was executed; and

correcting the predicted address if the address is mispredicted.

2. (Original) The method of claim 1, wherein storing the predicted address comprises programming the address into a read-only memory.

3-9. (Canceled)

10. (Currently Amended) The method of claim [[9]] 1, wherein correcting the predicted address comprises zeroing out the two least significant bits of the next micro-operation address.

11. (Original) The method of claim 1, further comprising storing the next micro-operation for use in an instruction pipeline.

12. (Original) The method of claim 11, wherein storing the next micro-operation comprises writing the micro-operation into a register.

13. (Currently Amended) A system comprising:

a first memory to store microcode, wherein the first memory is accessed at a next address to get a next micro-operation including at least two jump bits positioned as the two least significant bits of the next micro-operation;

a second memory to store predicted micro-operation addresses comprising a plurality of bits;

misprediction recovery logic coupled to the first memory to determine if the predicted address is correct and to determine a recovery address, the misprediction recovery logic to determine whether a jump was executed by checking the jump bits of the next micro-operation; and

a selector coupled to the first memory, the second memory, and the misprediction recovery, to select either the predicted address or the recovery address as the next address

at which to access the first memory based on the determination by the misprediction recovery logic as to whether the predicted address is correct.

14-18. (Canceled)

19. (Currently Amended) The system of claim **[[**18**]]** 13, wherein the misprediction recovery logic to determine the recovery address comprises the misprediction recovery logic to zero out the two least significant bits of the next address.

20. (Original) The system of claim 19, wherein the misprediction recovery logic to determine the recovery address further comprises the misprediction recovery logic to add the number of micro-operations per line to the next address.

21. (Original) The system of claim 13, further comprising a register coupled to the first memory to store the next micro-operation.

22 (Original) The system of claim 13, further comprising a register coupled to the first memory to store the next address for use by the misprediction recovery logic.

23. (Original) The system of claim 13, wherein the selector is a multiplexer.

24-30. (Canceled)